**ECE MS Comprehensive Exam – October 17, 2009**

**Depth/Topic: Computer Engineering (GRAD)**

Student Name: _______________________

PID: ______________________________

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**Overall Topic**

PASS / FAIL  

*(circle one)*

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This is a totally closed-book exam: No notes, books or magic genie are allowed.
CE: Question 1

(a) What logic function does the circuit below implement? I.e. \( Y = f(A,B) \); find \( f(.) \).

(b) Rank the following three logic styles: FPGA / cell-based design / PLA, according to three criteria. First rank them according to unit cost (cheapest first). Second, rank them according to flexibility (most flexible first). Third, rank them according to performance (highest first).

(c) What is the equation for the dynamic power dissipation of a circuit with total switched capacitance \( C \), supply voltage \( V \) and operating frequency \( f \)?
CE: Question 2

(a) What is the time constant of the RC chain shown below, using the Elmore delay model?

\[ N = 5 \]
\[ C_i = 1 \text{ pF} \]
\[ R_i = 1 \text{ k}\Omega \]

(b) Consider the metal trace running between points A and B, with dimensions \( x = 60 \mu\text{m}, y = 2 \mu\text{m}, z = 3 \mu\text{m} \). The resistance is measured to be 600 \( \Omega \).

What would the resistance be when \( x = 120 \mu\text{m}, y = 4 \mu\text{m}, z = 3 \mu\text{m} \)?

What is the value of the sheet resistance of this trace?
(a) Very concisely (1 or 2 sentences), describe the fundamental difference between a latch and a flip flop.

(b) Consider the circuit below. The latches have zero delay and hold time, but a setup time of 1 ns.

What is the maximum delay of combinational logic block 1 if it is allowed to maximally borrow time from combinational logic block 2?