Circuits Test: Show your work and give concise answers. Assume in the problems below (unless otherwise specified) that pn junction diodes have a dc voltage drop of 0.7 V when forward biased.

<table>
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<tr>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>Total Points</th>
</tr>
</thead>
</table>

In these problems, analyze the following circuits and show that you understand how to use these circuits. Express answers in the simplest form to receive full credit.

![Op-Amp Configurations](image)

1. Find the voltage transfer function for each of the circuits in Figure 1 assuming the op-amp gain is infinite. (15, 5 for each circuit)

2. Now assume that the op-amp has a gain given by $A(s) = 10^6/s$. What is the phase margin of each of the circuits in Figure 1? (15)

3. Now assume that the op-amp has an infinite gain, but an input offset voltage = 10 mV (that is, the output voltage is zero when the positive terminal of the op-amp input is 10 mV and the negative terminal is grounded). What is the dc output voltage of each of the circuits in Figure 1? (11)

4. What is the dc voltage $v_{out}$ of each of the three circuits in Figure 2? (9)
5. What is the small-signal gain of each of the circuits in Figure 3? 10 pts.

6. What is the d.c. voltage at the collector of the circuit of Figure 3? 5 pts.

7. What logical function do each of the circuits in Figure 4 perform? 15 pts.

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Figure 4. Logic Gates

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Circuits Test: Show your work and give concise answers.

<table>
<thead>
<tr>
<th>Analog (50)</th>
<th>Communications (50)</th>
<th>Total Points</th>
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**Analog:** In this problem, analyze the small-signal behavior of some common transistor configurations and show that you understand how to use these circuits. Express all answers in pole-zero form in the simplest form to receive full credit.

1.) Determine the unity current gain frequency for the first-order NMOS model in Fig. 1. Assume the source is grounded, a voltage source drives the gate, and the output is the drain. (5)

\[ f_T = \frac{1}{2\pi C_{gs}} \frac{g_m}{R_t} \]

2.) For the source follower stage in Fig. 2, derive the input impedance based on the first-order NMOS model. (5)

\[ Z_{in} = R_s + R_t + \frac{1}{sC_{gs}} (1 + g_m R_t) \]

3.) For the source follower stage in Fig. 2, derive the output impedance based model in Fig. 1. (10)

\[ Z_{out} = \frac{R_t}{1 + sC_{gs} R_s} \frac{1 + sC_{gs} R_t}{1 + sC_{gs} (R_s + R_t)} \]

4.) For the source follower stage, derive the voltage transfer function. (10)

\[ A_v = \frac{g_m R_t}{1 + sC_{gs} R_t} \frac{1 + sC_{gs} R_t}{1 + sC_{gs} R_t} \]

5.) What is the 3dB bandwidth of the source follower stage? (5)

\[ f_{3dB} \approx \frac{1}{2\pi} \frac{1 + g_m R_t}{R_t C_{gs}} \]

6.) For the common source stage, derive the voltage transfer function. (10)
\[ A_v = g_m R_d \frac{1}{1 + sC_{gs} R_s} \frac{1}{1 + sC_{l} R_d} \]

7.) If the first order transistor model included a gate-drain capacitance, Cgd, where would the zero be located in the common source voltage transfer function? (5)

\[ f_z = \frac{1}{2\pi C_{gd}} \]

 Problem 2: RF and Communication Circuits

Impedance Matching: The following questions refer to Fig. 1.

![Fig. 1. Impedance Matching Networks](image)

1) If \( Z_L = 40 + j30 \Omega \) and \( Z_o = 50 \Omega \), which impedance matching network would you use? Justify your answer. (5)

The real part of the load impedance is less than the source impedance. Therefore, the network on the left should be used.

2) Find the impedance, \( X \), and susceptance, \( B \), for the matching network. (15)

\[ Q = \sqrt{\frac{50}{40}} - 1 = \sqrt{0.25} = 0.5 \, , \, X + 30 = |QR| = 0.5 \cdot 40 = \pm 20 \rightarrow X = -10, -50 \]

\[ B = \frac{1}{\Im \{Z_L\} + X + \left(\frac{\Im \{Z_L\}}{20 + 40^2/20}\right)^2} = \frac{1}{100} = \frac{1}{100}, \frac{1}{20 - 40^2/20} = \frac{-1}{100} \]

3) Assume the matching network is not used and find the return loss as seen from the source in db. (5)

\[ \Gamma = \frac{Z_L - Z_o}{Z_L + Z_o} = \frac{-10 + j30}{90 + j30} = \frac{-900 + j2700 + j300 + 900}{8100 + 900} = \frac{j}{3} \]
\[ RL = 20 \log_{10} |\Gamma| = -20 \log_{10} (3) = -9.5 \text{dB} \]

**Communication Circuits:** The receiver chain is required for a new radio. It consists of an input attenuator, an RF amplifier, a SSB mixer, a bandpass IF filter, and a bandpass ADC.

<table>
<thead>
<tr>
<th>G₁ = 20dB</th>
<th>G₂ = 0dB</th>
<th>G₃ = 6dB</th>
<th>ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>NF₁ = 6dB</td>
<td>NF₂ = 10dB</td>
<td>NF₃ = 6dB</td>
<td>NF₄ = 30dB</td>
</tr>
</tbody>
</table>

**Fig. 2. Receiver Chain**

4) Your company is designing a receiver chain and has specified the building blocks in Fig. 2.
   What is the receive chain gain in dB? (5)
   \[ G = G₁ G₂ G₃ = 10 \cdot 0.5 = 5 \rightarrow 14 \text{dB} \]

5) What is the single sideband noise figure of the receive chain seen at the antenna? (10)
   \[ F = 2 + \left( F₁ - 1 \right) + \frac{F₂ - 1}{G₁} + \frac{F₃ - 1}{G₁ G₂} = 2 + 3 + \frac{10}{10} + \frac{4}{10} = 6.4 \rightarrow 8 \text{dB} \]

6) Now consider the RF amplifier in Fig. 3 that is used in your receiver chain. What is the IIP3 of the BJT amplifier? Assume \( V_T = 25 \text{mV} \). Remember that the Taylor series is
   \[ f(x) = f(a) + f'(x-a) + f''(x-a)/2 + f'''(x-a)/6 \quad \text{and} \quad \text{IIP3} = \left| \frac{4 g₁}{3 \beta₃} \right| \]

   \[ V_o = V_{cc} - I_c R₁ = V_{cc} - I_c e^{\pi/\gamma} R₁ \]
   \[ \text{IIP3} = \sqrt{\frac{4 \cdot 6 V_T^2}{3}} = 2\sqrt{2} V_T \approx 70 \text{mV} \]