University of California, San Diego

M.S. Exam: Computer Engineering

Fall 2011 Solutions

1. Consider two NMOS transistors connected in series between +5V and ground and supplied with the same Vg. Label the node connecting one transistor's drain to the other's source "V1," and assume $V_t = 0.7V$, $kp = 100\mu A/v^2$, $W = 20\mu m$, and $L = 0.5\mu m$.

a. Under what conditions is V1 > 0? **Vg > 0.7V**

b. List the three operating modes of a MOS transistor. Which mode acts like a variable resistor? **Cutoff; linear/triode; sat. linear**

When V1 > 0, we found that dV1/dVg ~ 0.3.

c. As Vg increases from 0 to 5V, into which operating modes does each transistor go? At approximately what Vg values do mode transitions occur?

Vg < 0.7: both in cutoff

Vg > 0.7 bottom in linear; top in saturation

Saturation equation gives equal current only at Vg = 0.7, right at edge of cutoff

2. Given up to 8 size 4 PMOS and 8 size 2 NMOS transistors and inputs A, B, C, and !C:

a. Build 2:1 multiplexer out of transmission gates.

W&H 4th ed. Fig 1.28

b. Build it out of tristate buffers

W&H 4th ed. Fig 1.29B

c. Built it out of logic gates

W&H 4th ed. Fig 1.29A

d.Write the algebraic function in either Boolean or HDL.

A.C + B.!C or **A.!C + B.C**

3. Consider the basic 6-transistor SRAM cell.

a) Describe how to write a "1" into it. **Pos. bit line = 1, neg. bit line = 0, then word line goes high**

b) Describe how to hold this value. **Turn off both side xstrs by keeping word line low**

c) Describe how to read the value we wrote. **Precharge both bit lines weakly high, bring word line high**

d) Qualitatively, what are the required relative strengths of the 3 pairs of transistors? **Strongest: word line (side) xstrs; weakest: tops of crossed inverters;**

4a. If the logic propagation delay between two flip-flops w/ t_s = 65ps, t_{cq} = 50ps, t_{cd} = 35ps, t_h = 30ps is 385ps, what is the maximum nominal clock frequency which may be applied, assuming a clock jitter of 1%?

See W&H website – soln # 10.1

prelim answer, no jitter: tcy = tpd + (tcq + ts) = 500

final soln, w/ +/-5ns jitter: 500 + 10 = 510ns

max freq = 1/510 = 1.96MHz

4b. For the same percentage clock jitter and the same logic propagation delay between two 2-phase transparent latches w/ t_s = 25ps, t_{dq} = 40ps, and all other parameters unchanged, what is the maximum nominal clock frequency which may be applied?

tcy = tpd + 2*tdq = 385 + 80 = 465ns

max freq = 1/465 = 2.15MHz)