University of California, San Diego
ECE Dept.
FA11 M.S. Comprehensive Exam
Computer Engineering (Grad)

Instructions:

All work to be done on the attached sheets. Write your name at the top of every sheet.

1. Consider two NMOS transistors connected in series between +5V and ground and supplied with the same Vg to their gates. Label the node connecting one transistor's drain to the other's source "V1," and assume $V_t = 0.7V$, $kp = 100\mu A/v^2$, $W = 20\mu m$, and $L = 0.5\mu m$.

1a. Under what conditions is V1 > 0?

1b. List the three operating modes of a MOS transistor. Which mode acts like a variable resistor?

1c. When V1 > 0, we found that dV1/dVg ~ 0.3. As Vg increases from 0 to 5V, into which operating modes does each transistor go? At approximately what Vg values do mode transitions occur?

2. Given up to 8 size 4 PMOS and 8 size 2 NMOS transistors and inputs A, B, C, and !C:

2a. Build 2:1 multiplexer out of transmission gates.

2b. Build it out of tristate buffers

2c. Built it out of logic gates

2d. Write the algebraic function in either Boolean or HDL.

3. Consider the basic 6-transistor SRAM cell.

3a. Describe how to write a "1" into it.

3b. Describe how to hold this value.

3c. Describe how to read the value we wrote.

3d. Qualitatively, what are the required relative strengths of the 3 pairs of transistors?

4a. If the logic propagation delay between two flip-flops w/ t_s = 65ps, t_{cq} = 50ps, t_{cd} = 35ps, t_h = 30ps is 385ps, what is the maximum nominal clock frequency which may be applied, assuming a clock jitter of 1%?

4b. For the same percentage clock jitter and the same logic propagation delay between two 2-phase transparent latches w/ t_s = 25ps, t_{dq} = 40ps, and all other parameters unchanged, what is the maximum nominal clock frequency which may be applied?