University of California, San Diego

M.S. Exam: Computer Engineering

Fall 2012

Name: _____

Instructions:

All work to be done on the attached sheets. Write your name at the top of every sheet.

1. Each bit cell (tap) of a masking correlator performs the function C = AND(M,NXOR(A,B)). (Verilog equivalent: assign C = M&(!A^B);)

1a. Design one tap using only NOT, NOR, and NAND gates.

1b. Design an area-efficient merged logic version of the same using PMOS and NMOS transistors.

1c. The other portion of a correlator counts the number of 1s (logic highs) produced by the various cells and reports this as a binary number. For a 3-tap correlator, how many output bits will be produced, and what common arithmetic logic block can be used to do this encoding?

2a. If the logic propagation delay between two flip-flops w/ t_s= 50ps, t_{cq} = 40ps, t_{cd} = 30ps, and t_h = 20ps is 360ps, what is the maximum nominal clock frequency which may be applied, assuming a clock jitter of 2%?

2b. What is the maximum allowable clock frequency if each flip-flop is replaced with a 2-phase transparent latch w/ t_s = 25ps and t_{dq} = 40ps? All other parameters aer unchanged.

3a. Draw an AOI22 standard cell, which comprises two 2-input AND gates feeding a 2-input NOR gate.

3b. Give three applications for this cell, which is a staple of every VLSI standard cell library.

3c. Design one in static logic, using 4 PMOS and 4 NMOS transistors.

3d. Size the transistors for equivalent resistance to a standard balanced inverter of unit size.

3e. What are the logical efforts of the respective inputs? Explain why all are or are not the same.

4a. Consider an NMOS device wired as a pass transistor. If $V_D = V_G = V_{DD}$, what is V_S?

4b. For the same device, if $V_D = V_G = 0$, what is V_S?

4c. For three such devices forming a serial channel, i.e., w/ S1 connected to D2, etc., what is V_S of each if all gates and the first drain are tied high?

4d. Repeat with three such devices in cascade, such that S1 is connected to G2, S2 is connected to G3, and all drains and G1 are connected to V_{DD}?