University of California, San Diego

M.S. Exam: CE Fall 2012

1. *Each bit cell (tap) of a masking correlator performs the function C = AND(M,NXOR(A,B)). (Verilog equivalent: assign C = M&(!A^B);)*

1a. *Design one tap using only NOT, NOR, and NAND gates.*

Start with W&H Fig 11.59 C=!(A&B), D=!(A&C), E=!(B&C), F=!(D&E), Y=!(!M|F)

Alt: C = !(A&B); D = !(A|B); E = !(!C|D); Y = !(!M|E)

1b. *Design an area-efficient merged logic version of the same using PMOS and NMOS transistors.*

Start w/ W&H Fig 11.59. Put PMOS driven by !M in series w/ existing 4PMOS; put NMOS driven by !M parallel to existing 4 NMOS

1c. *The other portion of a correlator counts the number of 1s (logic highs) produced by the various cells and reports this as a binary number. For a 3-tap correlator, how many output bits will be produced, and what common arithmetic logic block can be used to do this encoding?*

2; full adder

2a. *If the logic propagation delay between two flip-flops w/ t_s= 50ps, t_{pcq} = 40ps, t_{cd} = 30ps, and t_h = 20ps is 360ps, what is the maximum nominal clock frequency which may be applied, assuming a clock jitter of 2%?*

(1-0.02)/(t_{pcq} + t_{pd} + t_s) = 0.98/(40+360+50ps) = 0.98/450ps = 2.178GHz

2b. *What is the maximum allowable clock frequency if each flip-flop is replaced with a 2-phase transparent latch w/ t_s = 25ps and t_{dq} = 40ps? All other parameters are unchanged.*

Use W&H Eqn 10.5. Range of acceptable answers is 0.98/(40+360ps) for wide pulse to 0.98(40+360+25ps) for vanishingly narrow pulse = 2.45GHz to 2.31GHz.

3a. *Draw an AOI22 standard cell, which comprises two 2-input AND gates feeding a 2-input NOR gate.*

F=A&B, G=A&B, Y=!(F|G) Fig 9.4 in W&H 4th ed.

3b. *Give three applications for this cell, which is a staple of every VLSI standard cell library.*

XOR/NXOR; 2:1 mux; AOI21 w/ equal path delays; half-adder sum; NOR, NAND

3c. *Design one in static logic, using 4 PMOS and 4 NMOS transistors.*

W&H Fig 9.4 PMOS: E = A, B in parallel; F = C, D parallel; E, F in series

NMOS: I = A, B in series; J = C, D in series; I, J in parallel

3d. *Size the transistors for equivalent resistance to a standard balanced inverter of unit size.*

PMOS: W = 4; NMOS: W = 2 because 2 NMOS xstrs in series, likewise PMOS

3e. *What are the logical efforts of the respective inputs? Explain why all are or are not the same.*

(4+2)/3 = 6/3 Every input sees 4 from P plus 2 from N – all the same

4a. *Consider an NMOS device wired as a pass transistor. If $V_D = V_G = V_{DD}$, what is V_S?* **V_{DD}-V_{th}**

4b. *For the same device, if $V_D = V_G = 0$, what is V_S?* **0**

4c. *For three such devices forming a serial channel, i.e., w/ S1 connected to D2, etc., what is V_S of each if all gates and the first drain are tied high?* **All are V_{DD}-V_{th}**

4d. *Repeat with three such devices in cascade, such that S1 is connected to G2, S2 is connected to G3, and all drains and G1 are connected to V_{DD}?* **V_{DD}-V_{th}, V_{DD}-2V_{th}, V_{DD}-3V_{th}**