**University of California, San Diego**

M.S. Exam: Computer Engineering

Spring 2013

Name: ___________________________________

***Instructions:***

*All work to be done on the attached sheets. Write your name at the top of every sheet.*

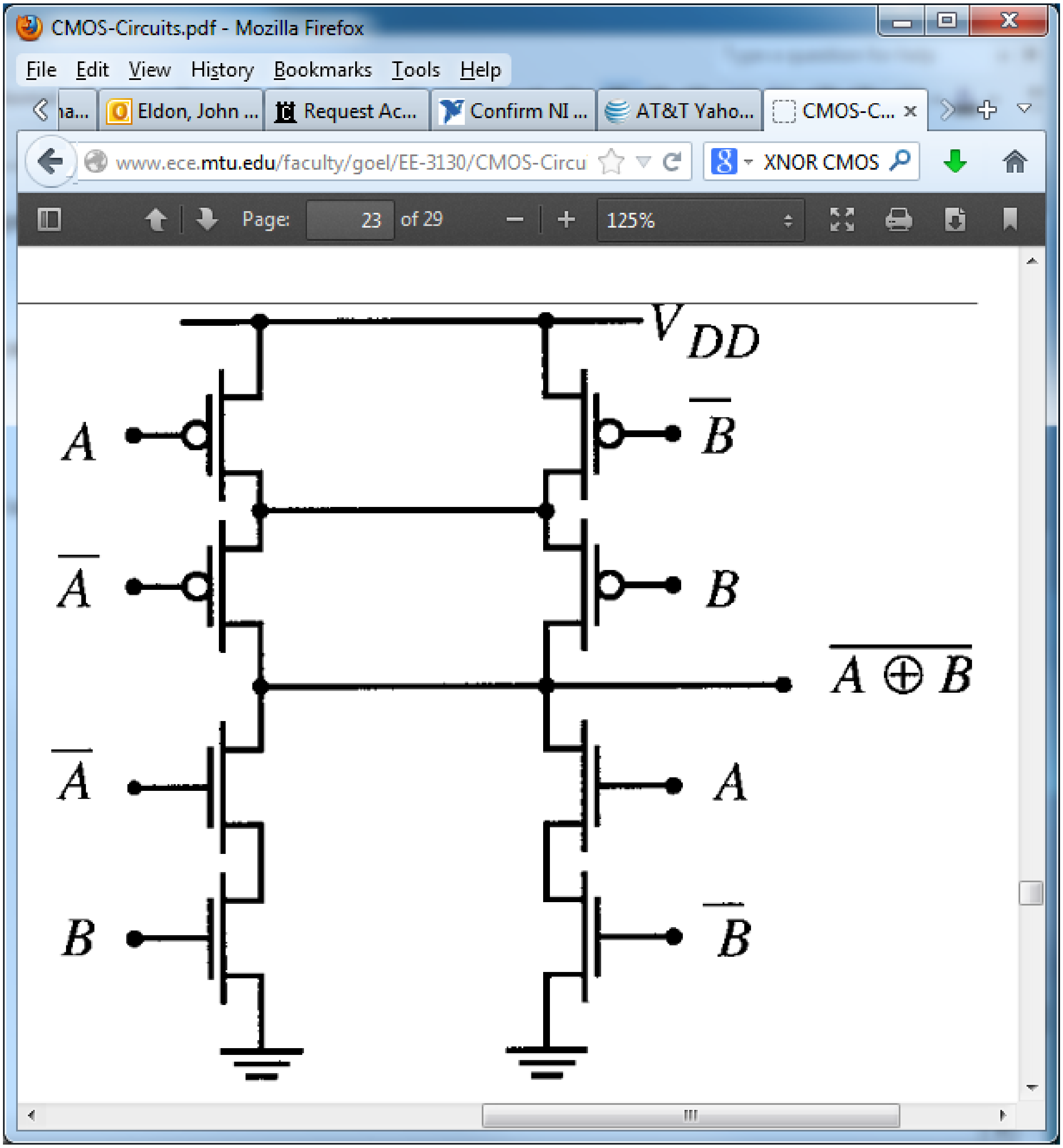
**1**. For an NMOS transistor with $V_{DS} = 1.0V$, kp = 100µA/$V^2$ and LAMBDA = 1/(Early voltage) = 0.01/V, if $I_D = 0.225mA$ when $V_{GS} = 0.9V$ and $I_D = 0.1mA$ when $V_{GS} = 0.8V$, find W/L and $V_t$.

**$I_D = 0.5*(V_{gs}-V_t)^2*100uA/V^2*(1.01)*W/L$**

**$I_{D1}/I_{D2} = 2.25$ ==> $V_{gt1}/V_{gt2} = 1.5$ ==> $V_t = 0.6V$**

**100uA = 0.5*($0.2^2$)*1.01*100*W/L => W/L = 2*0.99/0.04 = 49.5**

**2a**. Design an 8-transistor static CMOS NXOR (or XNOR) gate.



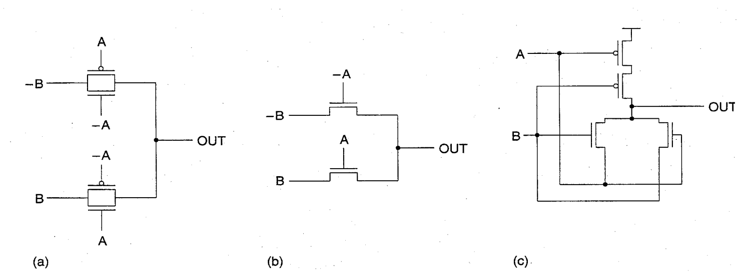

**2b**. If the N devices have W = 40 and L = 2, what should W and L of the P devices be for a 2:1 mobility ratio?

**W = 80, L = 2**

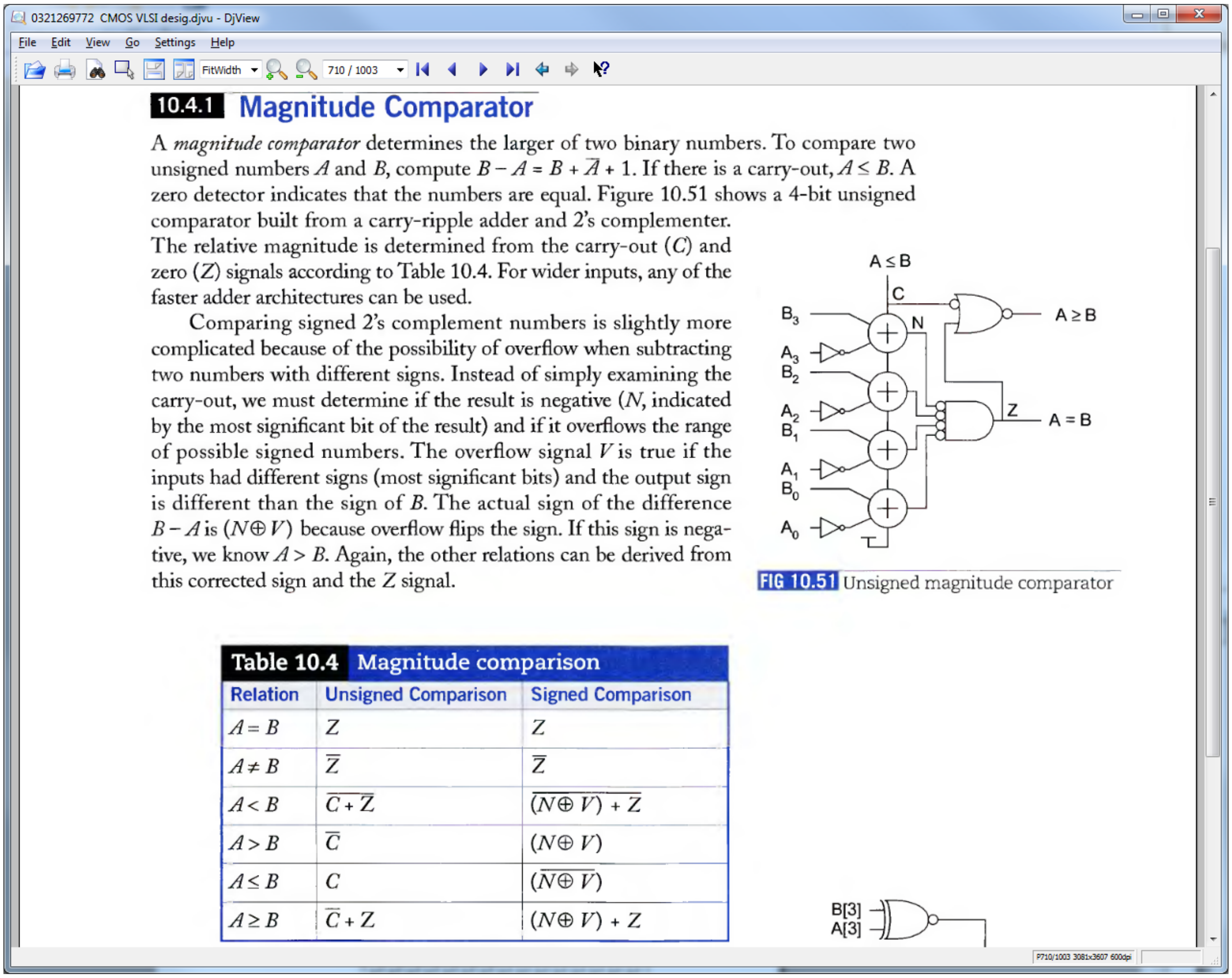
**2c**. Design the same function using 2 transmission gates and a static inverter.

**One solution is to follow A or B below with an inverter.**

# Complementary Pass-Transistor Logic



**3a**. Using combinations of static or pseudoNMOS AND and OR gates, design a comparator which accepts two unsigned 4-bit numbers and outputs three flags: A=B, A>B, and B<A.



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### 10.4.1 Magnitude Comparator

A *magnitude comparator* determines the larger of two binary numbers. To compare two unsigned numbers $A$ and $B$, compute $B - A = B + \overline{A} + 1$. If there is a carry-out, $A \le B$. A zero detector indicates that the numbers are equal. Figure 10.51 shows a 4-bit unsigned comparator built from a carry-ripple adder and 2's complementer. The relative magnitude is determined from the carry-out ($C$) and zero ($Z$) signals according to Table 10.4. For wider inputs, any of the faster adder architectures can be used.

Comparing signed 2's complement numbers is slightly more complicated because of the possibility of overflow when subtracting two numbers with different signs. Instead of simply examining the carry-out, we must determine if the result is negative ($N$, indicated by the most significant bit of the result) and if it overflows the range of possible signed numbers. The overflow signal $V$ is true if the inputs had different signs (most significant bits) and the output sign is different than the sign of $B$. The actual sign of the difference $B - A$ is $(N \oplus V)$ because overflow flips the sign. If this sign is negative, we know $A > B$. Again, the other relations can be derived from this corrected sign and the $Z$ signal.



FIG 10.51 Unsigned magnitude comparator

**Table 10.4 Magnitude comparison**

| Relation | Unsigned Comparison | Signed Comparison |
|---|---|---|
| $A = B$ | $Z$ | $Z$ |
| $A \ne B$ | $\overline{Z}$ | $\overline{Z}$ |
| $A < B$ | $\overline{C + Z}$ | $\overline{(N \oplus V) + Z}$ |
| $A > B$ | $\overline{C}$ | $(N \oplus V)$ |
| $A \le B$ | $C$ | $(\overline{N \oplus V})$ |
| $A \ge B$ | $\overline{C} + Z$ | $(N \oplus V) + Z$ |

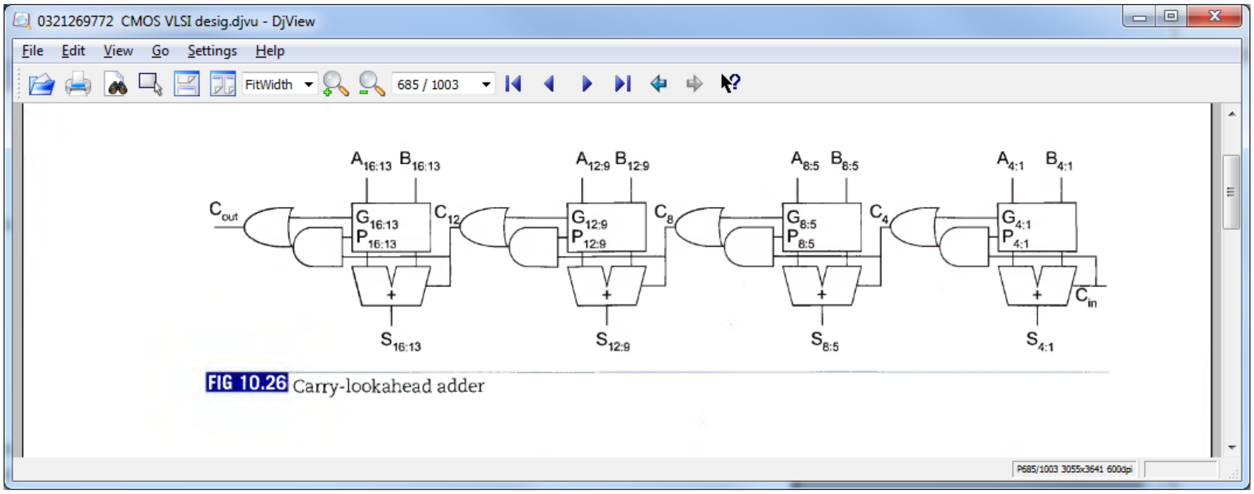


**3b.** Repeat for two's complement operands.

**Generate V using logic for which V = 1 iff $A_3$ != $B_3$ and $A_3$ = N**

**Accept AND(XOR($A_3$,$B_3$),XNOR($A_3$,N)) or AND(XOR($A_3$,$B_3$),XOR($B_3$,N))**

**4a**. Design a 16-bit two-operand carry lookahead adder using four 4-bit propagate-generate (PG) stages.




**4b**. Explain how a PG adder cell functions. Specifically: Under what conditions does the propagate flag go high? Under what conditions does the generate flag go high? How is a carry kill (P = G = 0) produced?

**Propagate Flag: High if $A_n$^$B_n$ = 1 for all n, i.e., A+B = 4'b1111**

**Generate Flag: A+B > 4'b1111**

**Carry kill: A+B < 4'b1111**