University of California, San Diego

M.S. Exam: Computer Engineering

Spring 2013

Name: _____

Instructions:

All work to be done on the attached sheets. Write your name at the top of every sheet.

1. For an NMOS transistor with V_{DS} = 1.0V, kp = 100μA/V^2 and LAMBDA = 1/(Early voltage) = 0.01/V, if I_D = 0.225mA when V_{GS} = 0.9V and I_D = 0.1mA when V_{GS} = 0.8V, find W/L and V_t.

2a. Design an 8-transistor static CMOS NXOR (or XNOR) gate.

2b. If the N devices have W = 40 and L = 2, what should W and L of the P devices be for a 2:1 mobility ratio?

2c. Design the same function using 2 transmission gates and a static inverter.

3a. Using combinations of static or pseudoNMOS AND and OR gates, design a comparator which accepts two unsigned 4-bit numbers and outputs three flags: A=B, A>B, and B<A.

3b. Repeat for two's complement operands.

4a. Design a 16-bit two-operand carry lookahead adder using four 4-bit propagate-generate (PG) stages.

4b. Explain how a PG adder cell functions. Specifically: Under what conditions does the propagate flag go high? Under what conditions does the generate flag go high? How is a carry kill (P = G = 0) produced?