University of California, San Diego

M.S. Exam: Computer Engineering

Fall 2014

Name: _____

Instructions:

All work to be done on the attached sheets. Write your name at the top of every sheet. 25 points/problem.

1. Consider the function F = (AB+C+DE)'

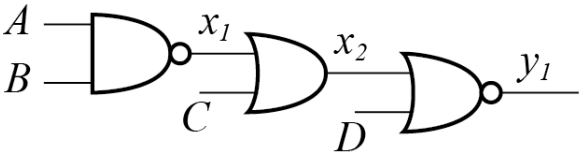
a. Design a transistor-level implementation of a single-stage static CMOS logic gate which minimizes the number of transistors. In your implementation, consider that input C is on the critical path, and inputs A and D are the next most important signals.

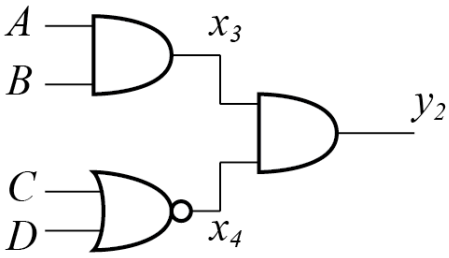
b. Show the sizes of the transistors needed to obtain the same worst-case drive as a unit inverter. (Assume P mobility is 1/2 that of N.)

c. Compute the logical effort of each of the five inputs.

d. Assuming all diffusion is fully contacted, estimate the Elmore delay when A, C, and D all fall from 1 to 0, while B and E remain at 1.

2. Consider the following two circuits:





2a) What are the logic functions implemented here?

2b) What is the probability of switching at each node given that $P_A = P_C = P_D = ½$, and $P_B = 1/4$?

2c) Which circuit features the lowest power consumption? Quantify your result. You can neglect the switching power of the inputs.

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3. Using NAND, NOR, and XOR gates, design a **comparator** which performs the following function:

if (**A - B = k**) **output = 1;**
else **output = 0;**

where inputs A, B, and k are 4-bit two's complement numbers and the output is a single bit. You may sketch the gates, write Verilog code, etc.

4. Consider a state machine comprising a flip-flop and a combinational circuit wired in a loop, i.e., the output of the flip-flop drives the combinational circuit, and the output of the combinational circuit drives the data input of the flip-flop.

For f_{clock} = 2GHz, and flip-flop parameters of:
t_{setup} = 65ps, t_{hold} = 30ps, $t_{clk\text{-}toQ}$ = 50ps, and $t_{contamination\_dly}$ = 35ps, compute:

4a) the maximum allowable $t_{propagation\_delay}$ for the combinational logic (0 clock jitter);

4b) repeat 4a) for jitter of up to +/- 50ps from one clock rising edge to the next

4c) the minimum allowable $t_{contamination\_delay}$ for the combinational logic (no jitter);

4d) repeat 4c) for +/-50ps jitter