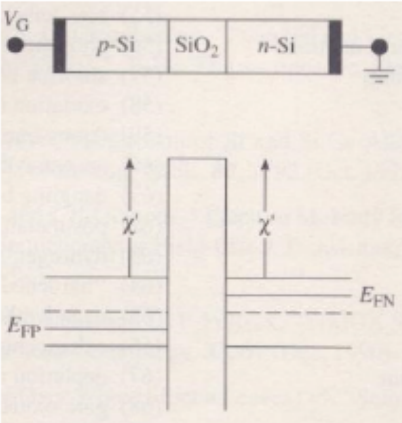
MS Exam, Spring 2014, Solid State Electronics (ECE 103)

1.

5. ~~(15 points, 3 points each)~~ The energy band diagram for a p-Si/SiO_2/n-Si capacitor (SOS-C) under flat-band conditions is given below. The SOS-C is ideal except for a non-zero work function difference. $T = 300$ K, N_A (p-side) = N_D (n-side) = 10^{15} cm^{-3}, $n_i = 10^{10}$ cm^{-3}, oxide thickness = 5×10^{-6} cm, and area $A_G = 10^{-3}$ cm^2.



(a) To achieve the pictured state, there must of course be a non-zero voltage applied to the SOS-C gate. What is it? Give both the polarity and magnitude of V_G. Give both a symbolic and numerical answer.

(b) Sketch the energy band diagram and the associated block charge diagram for the SOS-C when a *large positive* gate voltage (say $V_G > 5$V) is applied to the device.

(c) Same as (b) except now a *large negative* voltage is applied to the gate.

(d) Make a sketch of the *high-frequency* C- V_G characteristic to be expected. Explain how you arrived at your sketch.

(e) Determine the *minimum* capacitance exhibited by the device. Give both a symbolic and numerical answer.

2.

7. ~~(9 points, 3 points each)~~ Apply constant-field scaling to the ideal current-voltage relations of MOSFETs in both the saturation and nonsaturation bias region. Assume the scaling factor $k = 0.6$, e.g., the new gate length L is now $0.6\,L$.

(a) How does the drain current scale in each bias region? Explain.

(b) How does the power dissipation per device scale in each bias region? Explain.

(c) Why is it important to develop "high κ" dielectric material to replace SiO_2? κ here means dielectric constant (not the k above).