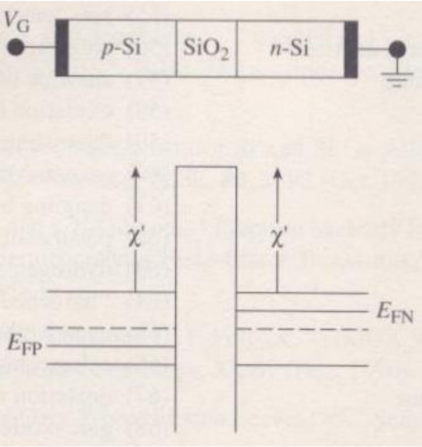
MS Exam, Spring 2014, Solid State Electronics (ECE 103)

~~5. (15 points, 3 points each)~~ 1. The energy band diagram for a *p*-Si/SiO_2/*n*-Si capacitor (SOS-C) under flat-band conditions is given below. The SOS-C is ideal except for a non-zero work function difference. $T = 300$ K, N_A (*p*-side) = N_D (*n*-side) = 10^{15} cm^{-3}, $n_i = 10^{10}$ cm^{-3}, oxide thickness = 5×10^{-6} cm, and area $A_G = 10^{-3}$ cm^2.



(a) To achieve the pictured state, there must of course be a non-zero voltage applied to the SOS-C gate. What is it? Give both the polarity and magnitude of V_G. Give both a symbolic and numerical answer.

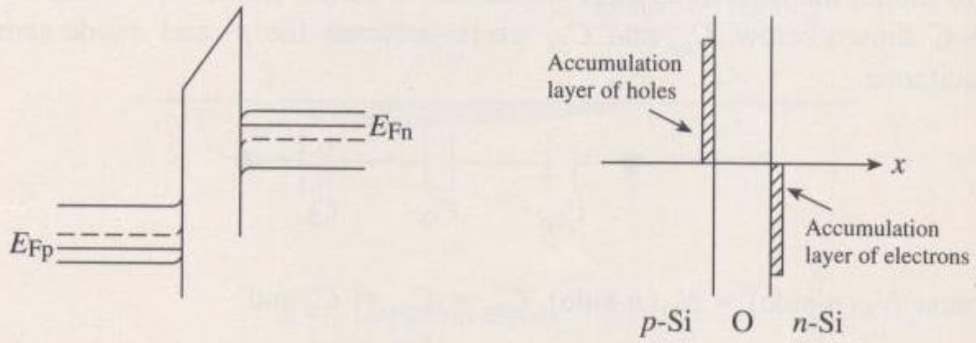
(b) Sketch the energy band diagram and the associated block charge diagram for the SOS-C when a *large positive* gate voltage (say $V_G > 5$V) is applied to the device.

(c) Same as (b) except now a *large negative* voltage is applied to the gate.

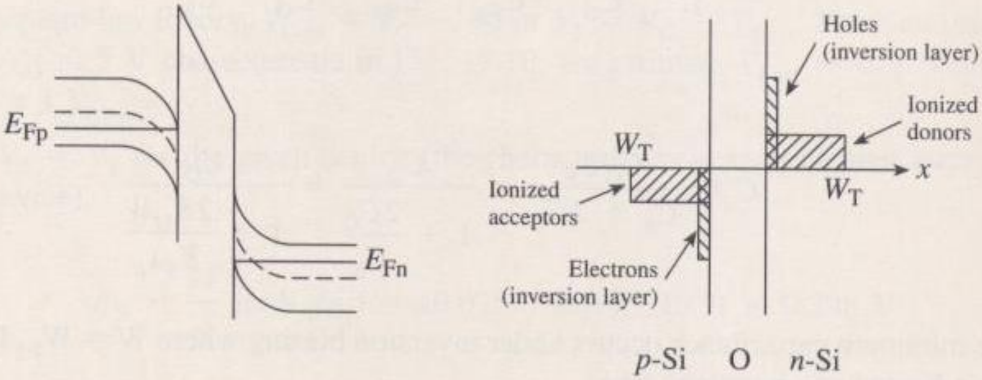
(a) $$V_G = \frac{1}{q}(E_{FN} - E_{FP}) = \frac{1}{q}[(E_{FN} - E_i) + (E_i - E_{FP})] = \frac{kT}{q}[\ln(N_D/n_i) + \ln(N_A/n_i)]$$

$$= 2(0.0259)\ln(10^{15}/10^{10}) = \mathbf{0.596\ V}$$

(b)

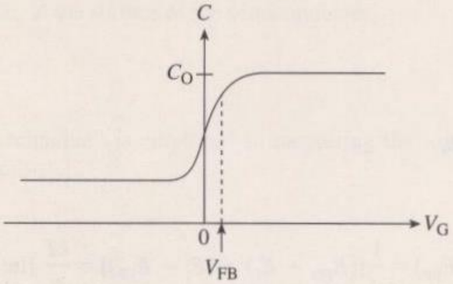


(c)

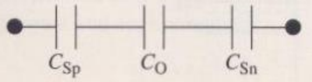


(d) Make a sketch of the *high-frequency* C- V_G characteristic to be expected. Explain how you arrived at your sketch.

(d) When $V_G > 0$, both semiconductor components are accumulated. Thus C approaches C_O at large positive gate biases. When $V_G < 0$, the two semiconductors components first deplete and then invert. Inversion occurs at the same bias voltage for the two sides of the SOS-C because $N_A(p\text{-side}) = N_D(n\text{-side})$. The high-frequency capacitance is therefore expected to smoothly decrease to C_{min} at large negative biases. As sketched below, the deduced characteristic should look very similar to a standard n-bulk high-frequency MOS-C C–V curve.



(e) Reflecting on the answers to previous parts of the problem, particularly part (c), we are led to model the SOS-C as three capacitors in series. In the equivalent circuit for the SOS-C shown below, C_{Sp} and C_{Sn} are respectively the p- and n-side semiconductor capacitance.



Because $N_A(p\text{-side}) = N_D(n\text{-side})$, $C_{Sp} = C_{Sn} = C_S$ and

$$\frac{1}{C} = \frac{1}{C_O} + \frac{1}{C_{Sp}} + \frac{1}{C_{Sn}} = \frac{1}{C_O} + \frac{2}{C_S}$$

or

$$C = \frac{C_O C_S}{C_S + 2C_O} = \frac{C_O}{1 + \dfrac{2C_O}{C_S}} = \frac{C_O}{1 + \dfrac{2K_O W}{K_S x_o}}$$

The minimum capacitance occurs under inversion biasing where $W = W_T$. Performing the indicated computations gives

(e) Determine the *minimum* capacitance exhibited by the device. Give both a symbolic and numerical answer.

$$\phi_F = \frac{kT}{q}\ln(N_A/n_i) = (0.0259)\ln(10^{15}/10^{10}) = 0.298\ \text{V}$$

$$W_T = \left[\frac{2K_S\varepsilon_0}{qN_A}(2\phi_F)\right]^{1/2} = \left[\frac{2(11.8)(8.85\times10^{-14})(0.596)}{(1.6\times10^{-19})(10^{15})}\right]^{1/2} = 8.82\times10^{-5}\ \text{cm}$$

$$C_O = \frac{K_O\varepsilon_0 A_G}{x_o} = \frac{(3.9)(8.85\times10^{-14})(10^{-3})}{(5\times10^{-6})} = 69.0\ \text{pF}$$

and

$$C_{min} = \frac{C_O}{1 + \dfrac{2K_O W_T}{K_S x_o}} = \frac{69.0}{1 + \dfrac{2(3.9)(8.82\times10^{-5})}{(11.8)(5\times10^{-6})}} = \mathbf{5.45\ pF}$$

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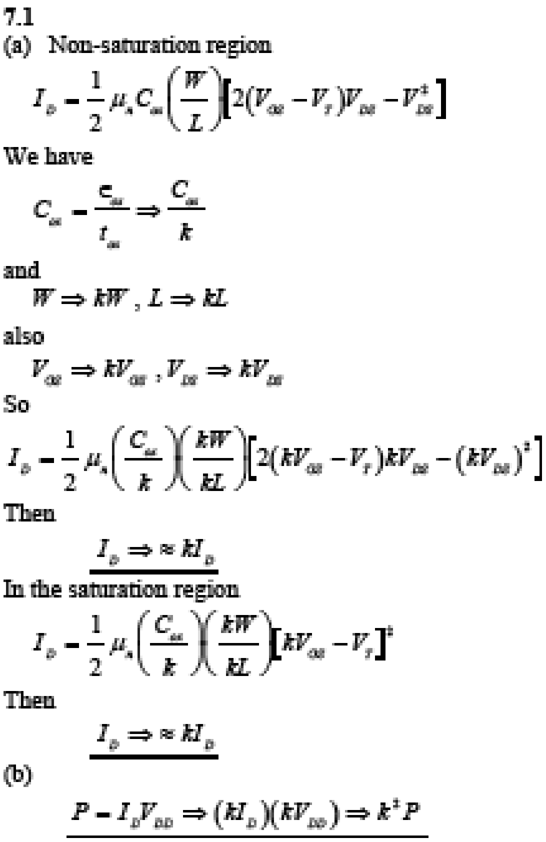
~~(9 points, 3 points each)~~ 2. Apply constant-field scaling to the ideal current-voltage relations of MOSFETs in both the saturation and nonsaturation bias region. Assume the scaling factor *k* = 0.6, e.g., the new gate length *L* is now 0.6 *L*.

(a) How does the drain current scale in each bias region? Explain.

(b) How does the power dissipation per device scale in each bias region? Explain.

(c) Why is it important to develop "high *κ*" dielectric material to replace SiO_2? *κ* here means dielectric constant (not the *k* above).

C = κ/d. The ultimate limit of *d* is one or two atomic layers, and the practical limit to have a continuous film may be several times higher. If κ is high, *d* can be thicker, which is more practical.



7.1

(a) Non-saturation region

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)\left[2(V_{GS}-V_T)V_{DS}-V_{DS}^2\right]$$

We have

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \Rightarrow \frac{C_{ox}}{k}$$

and

$$W \Rightarrow kW\ ,\ L \Rightarrow kL$$

also

$$V_{GS} \Rightarrow kV_{GS}\ ;\ V_{DS} \Rightarrow kV_{DS}$$

So

$$I_D = \frac{1}{2}\mu_n\left(\frac{C_{ox}}{k}\right)\left(\frac{kW}{kL}\right)\left[2(kV_{GS}-V_T)kV_{DS}-(kV_{DS})^2\right]$$

Then

$$\underline{I_D \Rightarrow \approx kI_D}$$

In the saturation region

$$I_D = \frac{1}{2}\mu_n\left(\frac{C_{ox}}{k}\right)\left(\frac{kW}{kL}\right)\left[kV_{GS}-V_T\right]^2$$

Then

$$\underline{I_D \Rightarrow \approx kI_D}$$

(b)

$$\underline{P = I_D V_{DD} \Rightarrow (kI_D)(kV_{DD}) \Rightarrow k^2 P}$$