University of California, San Diego

ECE M.S. Exam: Computer Engineering (ECE260A)

Fall 2013

NAME: _____

- Please do all work on the attached sheets.
- Write your name at the top of every sheet.
- Assume that the four questions are equally weighted.

Question 1.

(a) Design a two-transistor **NON**-inverting buffer.

(b) What are its two performance disadvantages with respect to an inverting buffer?

Question 2.

For inputs A, B, and S and output Y:

(a) Build a 2:1 multiplexer out of CMOS transmission gates.

(b) Build it using CMOS tristate buffers.

(c) Build it out of CMOS static logic gates.

(d) Write the algebraic function in either Boolean or HDL.

Question 3.

Consider a 4-bit-wide 4-input adder which computes E[N-1:0] = A[3:0]+B[3:0]+C[3:0]+D[3:0].

(a) Assuming unsigned arithmetic, what is the minimum value of N which prevents overflow?

(b) Repeat 3(a) for two's complement arithmetic.

(c) Build the two's complement version of this adder out of two-input carry propagate adders in the fastest topology.

(d) Build the two’s complement version using carry-save adders.

Question 4.

(a) A block of combinational logic connects the output of one flip-flop to the input of another. If the logic propagation delay of this block is 385*ps* and the flip-flop parameters are t_{setup} = 65*ps*, t_{pcq} = 50*ps*, t_{cd} = 35*ps*, t_{hold} = 30*ps*, what is the maximum nominal clock frequency which may be applied, assuming a clock jitter of 1%?

(b) For the same percentage clock jitter and the same logic propagation delay between two 2-phase transparent latches with t_{setup} = 25*ps*, t_{pdq} = 40*ps*, and all other parameters unchanged, what is the maximum nominal clock frequency which may be applied?