ECE164/ECE264A Problem

Each problem below relates to the following amplifier circuit. In solving each part, you may assume that

(i) all small signal model capacitances except for C_C and C_L may be neglected (although you may neglect it here, in practice C_{gs6} would also be significant),

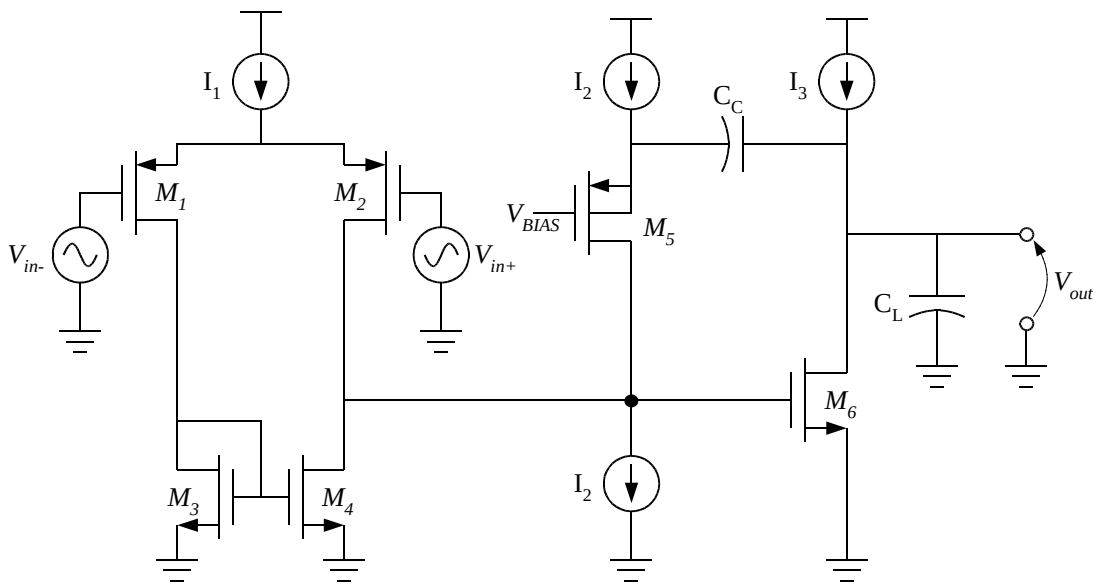
(ii) all transistors are in saturation,

(iii) the differential to single ended amplifier stage consisting of the I_1 current source and transistors M_1-M_4 has a differential mode gain of $g_{m1}R_1$ and an output impedance of R_1 where $R_1 = r_{ds2} \parallel r_{ds4}$,

(iv) all the current sources are ideal,

(v) $r_{ds_i} \gg 1/g_{m_j}$ for all values of i and j, and

(vi) r_{ds5} may be neglected.



1. Assuming that one of the poles of the differential-mode amplifier gain is dominant, derive an approximate expression for the 3 dB bandwidth of the amplifier.

2. Derive and draw a block diagram corresponding to the amplifier for a differential input signal, $v_{id}(s) = v_{in+}(s) - v_{in-}(s)$. The block diagram should have an input of $v_{id}(s)$, and three nodes corresponding to voltages $v_{gs6}(s)$, $v_{s5}(s)$, and $v_{out}(s)$.

3. Derive an expression for the differential-mode gain of the amplifier. Is your answer consistent with that of Problem 1?

4. The denominator of the gain you derived in response to Problem 3 above should have the form $1 + \beta s + \alpha s^2$ where α and β depend upon circuit parameters. You may assume that the poles are sufficiently far apart that $1 + \beta s + \alpha s^2 \approx (1 + s\beta)(1 + s\alpha/\beta)$. Using this approximation, write expressions for the poles and zero of the differential amplifier gain.