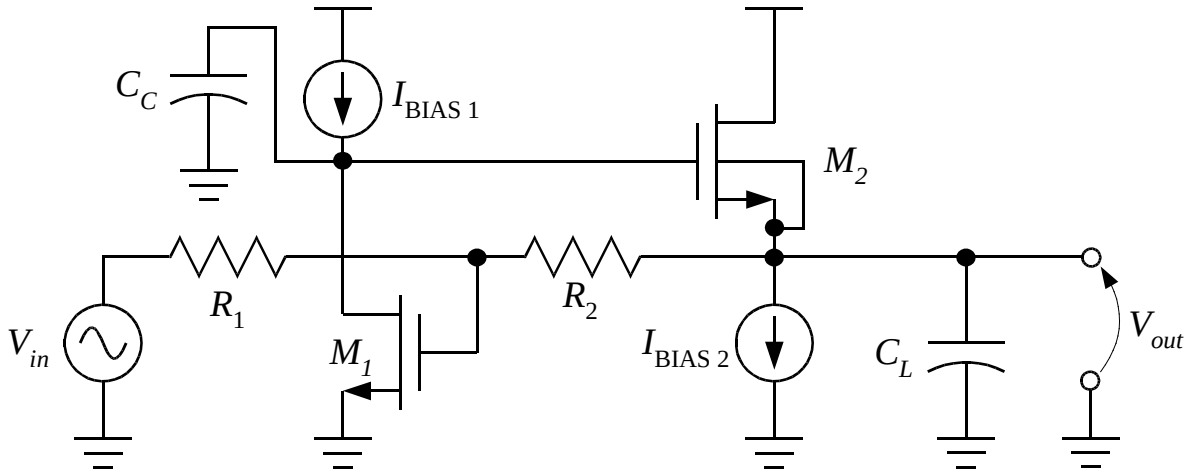
M.S. Comprehensive Exam – Spring 2013
Electronic Circuits & Systems ECE164/ECE264A

The following problems relate to the amplifier circuit shown below. In solving each problem, you may assume that

(i) Capacitances C_C and C_L are sufficiently large that the small-signal transistor model capacitances may be neglected,
(ii) all transistors are in saturation,
(iii) all the current sources are ideal, and
(v) $r_{ds_i} \gg 1/g_{m_j}$ for all values of i and j.



Solve any 4 of the following 5 problems and clearly indicate which problems you chose to solve. If you provide solutions or partial solutions to all the problems and do not indicate which four of your solutions should be graded, the grader will only grade Problems 1-4.

1) Derive a block diagram of the circuit with input $v_{in}(s)$, output $v_{out}(s)$, and nodes corresponding to $v_{gs1}(s)$ and $v_{ds1}(s)$. Do not include any other nodes in your block diagram.

2) Derive an expression for $A_v(s) = v_{out}(s)/v_{in}(s)$.

3) Derive an expression for the loop gain, $T(s)$, directly from the small-signal model representation of the circuit (not using the block diagram you derived).

4) Suppose $R_1 = 2$ kΩ, $R_2 = 8$ kΩ, $g_{m1} = 2\cdot10^{-3}\ \Omega^{-1}$, $r_{ds1} = 200$ kΩ, $g_{m2} = 10^{-4}\ \Omega^{-1}$, $r_{ds2} = 1$ MΩ, $C_C = 300$ fF, and $C_L = 3$ pF. Calculate the phase margin of the circuit.

5) Choose a new value for C_C that results in a phase margin of 65 degrees.