MS Exam, Fall 2012, Solid State Electronic Devices (ECE 230A-B)

ECE230A:

1. III-V compound semiconductor GaAs has two families of cleavage planes (110) and $(1\bar{1}0)$. You can cut the crystal along these two planes to create mirror-like facets. This is how semiconductor lasers are fabricated (i.e. using the cleaved planes as reflecting mirrors). For a (211) GaAs wafer, find

   a. the cleavage plane(s) that can cut through the (211) wafer with a mirror-like facet,
   b. the plane that is normal to both the (211) plane and the cleavage plane(s) in (a),
   c. what is the lattice structure of GaAs and InP?
   d. The lattice constant for GaAs is 5.65 Å. Find the interplane distances for (111) planes and (211) planes,
   e. Calculate the bond length of GaAs crystal.

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ECE 230B:

Assume silicon, room temperature, complete ionization.

1. For an abrupt n^+-p diode in Si, the n^+ doping is 10^{20} cm^{-3}, the p-type doping is 3×10^{16} cm^{-3}. Assume room temperature and complete ionization.

(a) Draw the band diagram at zero bias. Indicate $x = 0$ as the boundary where the doping changes from n^+ to p. Also indicate where the Fermi level is with respect to the midgap.

(b) Write the equation and calculate the built-in potential.

(c) Write the equation and calculate the depletion width.

(d) Will the built-in potential increase or decrease if the temperature goes up and why?

2. Consider an n-channel MOSFET with 20 nm thick gate oxide and uniform p-type substrate doping of 10^{17} cm^{-3}. The gate work function is that of n^+ Si.

(a) What is the threshold voltage? Sketch the band diagram at threshold condition, $\psi_s = 2\psi_B$.

(b) What is the threshold voltage if a reverse bias of 1 V is applied to the substrate? Sketch the band diagram at threshold.