Logic Design

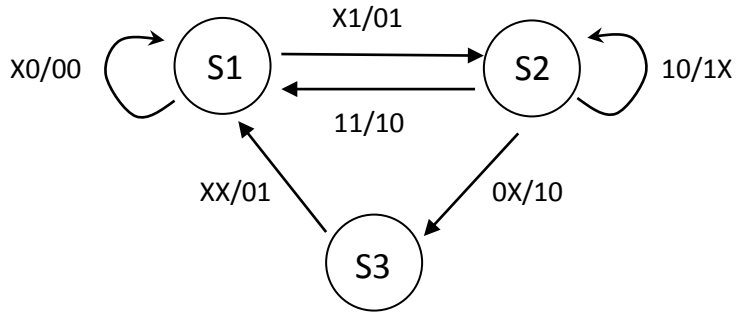
M.S. Comprehensive Exam Spring 2013

1. Below is the state diagram for a three-state, two-input, two-output state machine.

(a) Fill in the one-hot transition table using the information in the state diagram. (5 points)

Input: AB

Output: XY



Next State	Present State	Condition	Output X	Output Y
S1	S1			
S1	S2			
S1	S3			
S2	S1			
S2	S2			
S3	S2			

(b) Determine the flip-flop input equation and output equation. (5 points)

D_{S1}=

D_{S2}=

D_{S3}=

X=

Y=

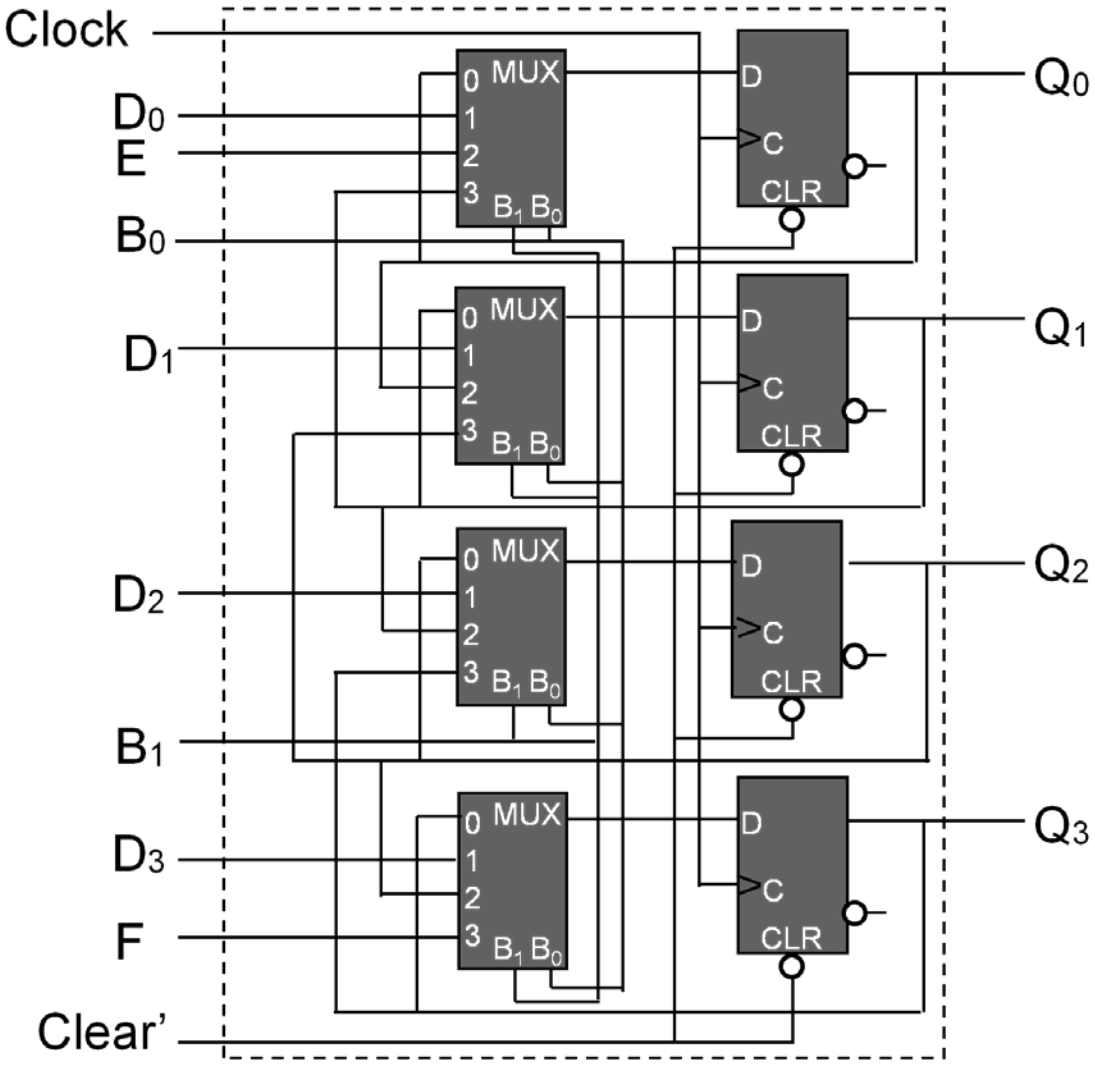
2. The following is the logic diagram of a bi-directional shift register with parallel load. The current states for $Q_3Q_2Q_1Q_0$ are 0011. The input values for D_3, D_2, D_1, D_0, E, F are fixed, i.e., D_3=0, D_2=1, D_1=0, D_0=1, E=1, F=0. (20 points total; 5 points each)

(a) If B_1=0, B_0=0, what is the next pattern for $Q_3Q_2Q_1Q_0$?

(b) If B_1=0, B_0=1, what is the next pattern for $Q_3Q_2Q_1Q_0$?

(c) If B_1=1, B_0=0, what is the next pattern for $Q_3Q_2Q_1Q_0$?

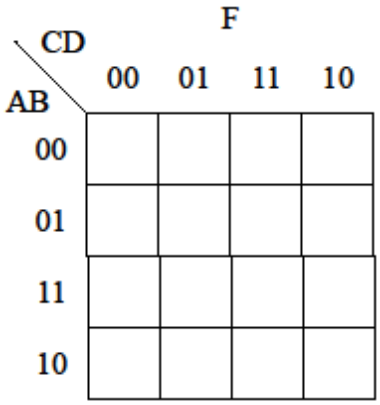
(d) If B_1=1, B_0=1, what is the next pattern for $Q_3Q_2Q_1Q_0$?



3. Two-level logic minimization (10 points total; 5 points each)

$$F(A, B, C, D) = \sum m(0,2,4,6,14,15)$$

$$d(A, B, C, D) = \sum m(1,7,8,11)$$



a) Identify all the prime and essential prime implicants.

Prime	Essential

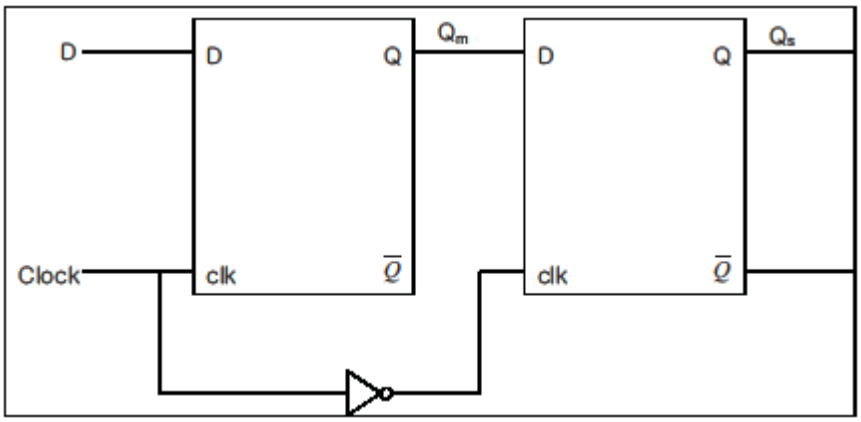
b) Find the minimum two-level logic implementation.

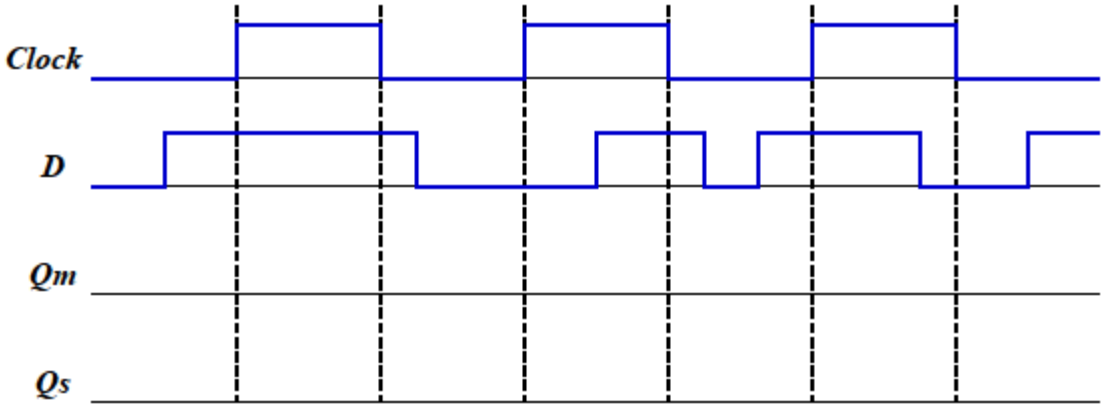
4. Different kinds of flip-flops (10 points total; 5 points each)

a) Fill in the excitation tables for J-K and D flop-flops.

Q	Q+	J	K	D
0	0			
0	1			
1	0			
1	1			

b) Complete the timing diagram for the following circuit. Note that the Ck inputs on the two flip-flops are different.





5. Design of two-level circuits using NAND and NOR gates

$$\mathrm{F(a, b, c, d)} = a'bd + ac'd$$

a) Find a two-level NAND gate circuit implementation. (You may use inverted inputs, i.e., a', b' etc.) (10 points)

b) Find a two-level NOR gate circuit implementation. (You may use inverted inputs, i.e., a', b' etc.) (10 points)

6. A sequential circuit has one input and one output. The output becomes 1 and remains 1 thereafter when at least two 0's ***and*** at least two 1's have occurred as inputs, regardless of the order of occurrence (otherwise, the output becomes 0). Draw a state graph (Moore type) for the circuit (nine states are sufficient). (20 points)

Example sequence)

input: 000000010000100011001111

output: 000000000000111111111111