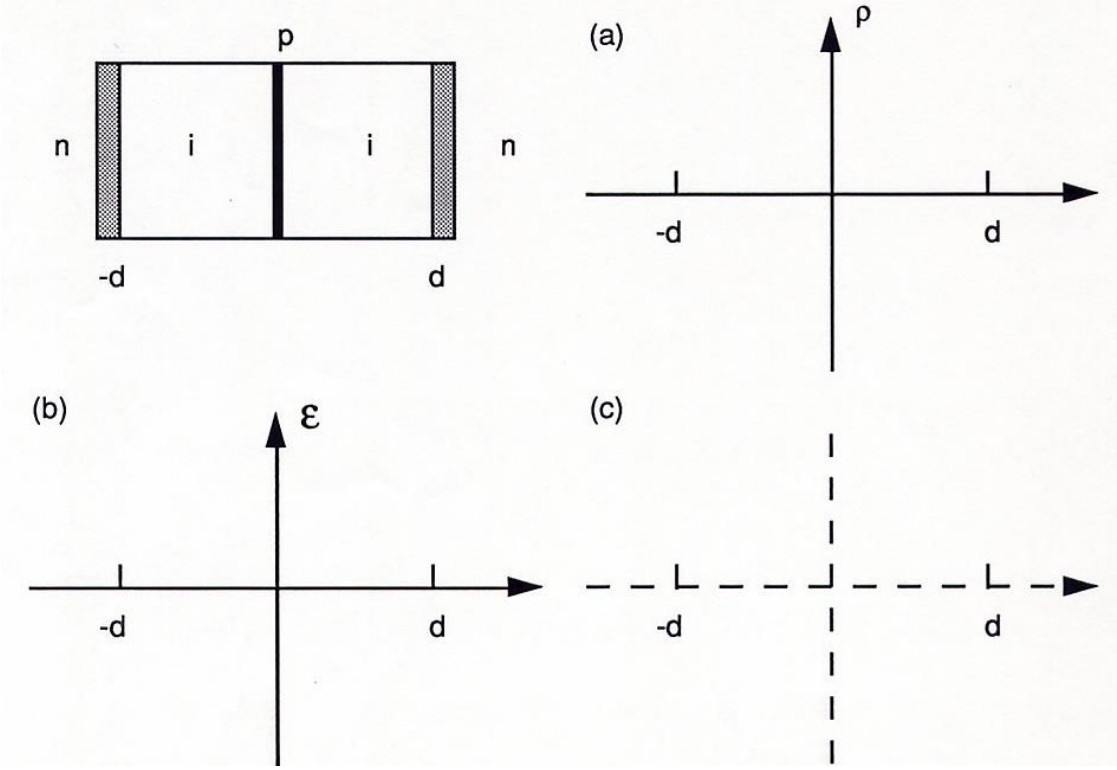
SOLID STATE ELECTRONICS – ECE 103
M.S. COMPREHENSIVE EXAM SPRING 2013

1. Semiconductor fundamentals.
   (a) Explain what the effective mass approximation is in semiconductor physics.

   (b) You have an *n*-type Si sample with one end heavily doped so that the carrier concentration is 10 times greater than the lightly doped end. You measure the voltage across the sample. Is the heavily doped end positive, negative, or the same (zero volts) as the lightly doped end? Explain.

2. In an *n-i-p-i-n* structure, the *p*-layer in the middle is very thin and the concentration of acceptors N_A in the *p*-layer is relatively small—so that the *p*-layer is totally depleted—and the doping level of the *n*-layer N_D is very large—so that the depletion regions in the *n*-type region is very thin and can be neglected.

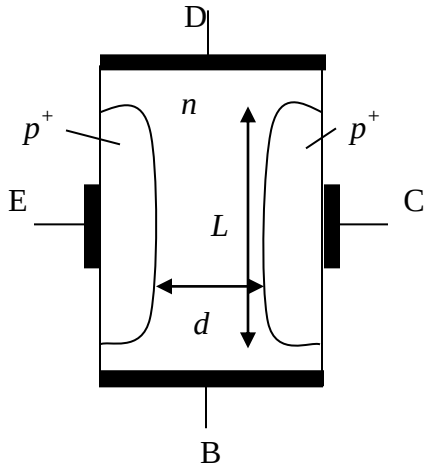


(a) Sketch the space-charge distribution.

(b) Sketch the electric-field distribution.

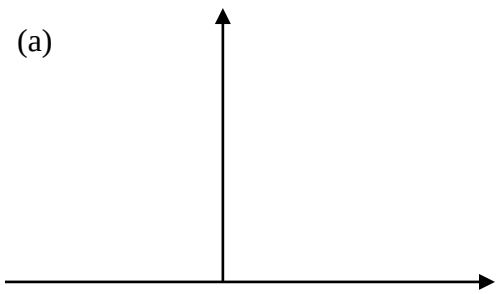
(c) Sketch the conduction and valence band energy diagram.

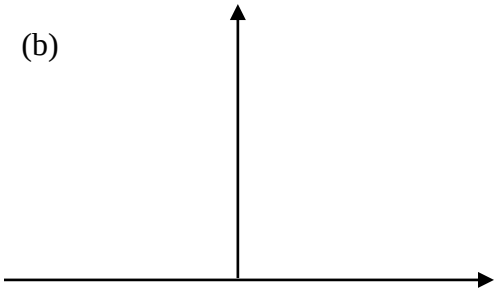
3. The figure below shows a device, which might be called a composite transistor. It is formed from a uniformly doped *n*-type bar. Ohmic contacts are made to the top and bottom of the bar and are connected to the outside world through leads D and B, respectively. p^+n abrupt junctions are formed on the two sides of the bar and are connected to the outside world through contacts E and C, and shown in the figure. d is the separation between the two p^+ regions and L is the lateral length of the p^+ regions. *To receive full credit you must indicate your reasoning* in addition to answering each of the following.



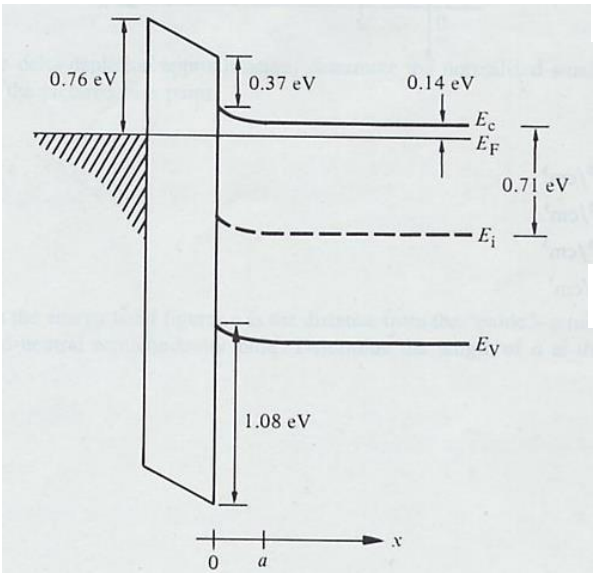
(a) *Given:* D-B tied together; $d << L_p$, where L_p is the minority carrier diffusion length in the *n*-region; $V_{EB} > 0$; $V_{CB} < 0$.
Problem: Sketch the current I_C flowing out of the C contact as a function of V_{CB} if I_E is held constant at various different values.

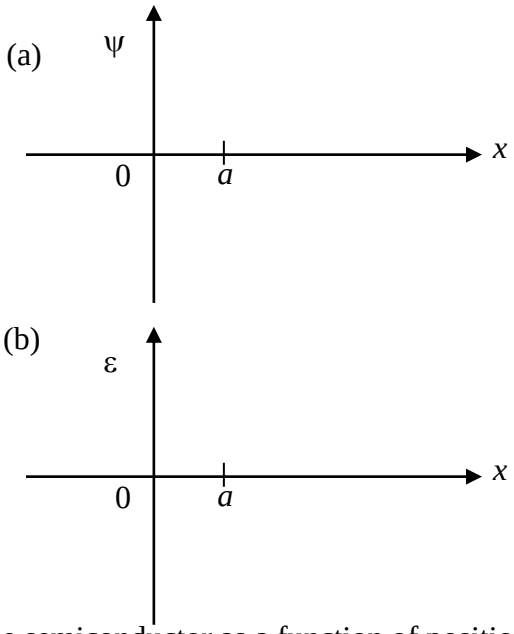
(b) *Given*: D-B tied together; E-C tied together; $d >> L_p$.
Problem: Sketch the current into the E-C leads as a function of the voltage applied from E-C to D-B.





4. A totally dimensioned energy band diagram for an M"O"S capacitor fabricated in a research laboratory is shown below. (The "O" is actually ZnSe and the semiconductor is GaAs.) The device is maintained at 300 K. It has also been established that there are no "oxide" charge nor interface traps. You can answer the questions by inspection of the diagram.





(a) Sketch the electrostatic potential ψ inside the semiconductor as a function of position. Let ψ = 0 in the semiconductor bulk.

(b) Sketch the electric field inside the semiconductor as a function of position.

(c) Do equilibrium conditions prevail *inside the semiconductor*? _____

(d) What is V_G? _____

(e) For the pictured condition, is the M"O"S capacitor in accumulation, depletion, or inversion mode? _____

(f) What is the metal-semiconductor work function difference? _____

(g) What voltage must be applied to the gate to achieve flat band condition? _____

5. MOSFET.

(a) The oxide thickness in an *n*-channel MOSFET is decreased, how would the threshold voltage be affected (decrease, the same, or increase)? Explain.

(b) If another metal with a larger work function is used as the gate for an *n*-channel MOSFET, how would the threshold voltage be affected (decrease, the same, or increase)? Explain.