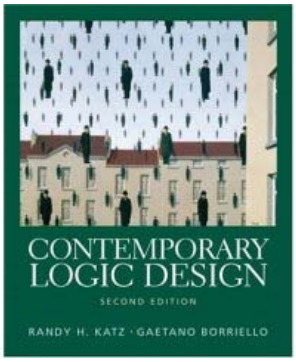
Revision 6/11/2008

MS Comprehensive Exam: Logic Design

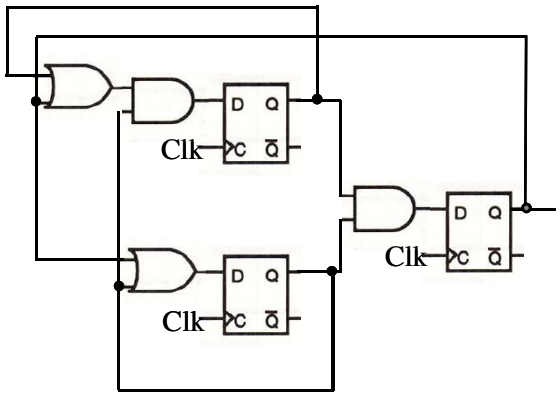
On the MS preliminary exam, there will be one question on logic design. This question will be at the level that is considered typical of an upper division undergraduate course on this topic, e.g. CSE140 taught here at UCSD, which uses the textbook "Contemporary Logic Design," 2nd Ed., R. Katz, G. Borriello, ISBN 0201308576. Please refer to the class website for information on the syllabus:
http://www.cs.ucsd.edu/classes/sp08/cse140/



First Name: Last Name: PID:

Problem 1. (10 points)
Determine the maximum frequency of the clock, given:

T_{setup} = 2ns
T_{pd} = 2ns
T_{hold} = 1.5ns
$T_{AND/OR}$ = 1ns (AND/OR gates delay)



Solution:
Critical path: OR -> AND -> D-FF:

$T_{period} > T_{pd} + T_{OR} + T_{AND} + T_{setup} = 2+1+1+2=6ns$

Frequency < 1/6ns

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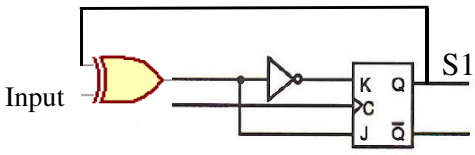
Problem 7. (15 points)
Using the following state transition table, implement the next state output, *S1+*, using *J-K flip-flops* with minimal logic gates.

I (Input)	Current state S1	S0	Next state S1+	S0+	Output
0	0	0	0	1	0
0	0	1	0	0	0
0	1	0	1	1	0
0	1	1	1	0	1
1	0	0	1	1	0
1	0	1	1	0	1
1	1	0	0	1	0
1	1	1	0	0	0

Solution:
Using K-map, the functions of J and K that are required to implement S1+ are shown in the following:

$K^+ = (I \oplus S1)'$
$J^+ = (I \oplus S1)$



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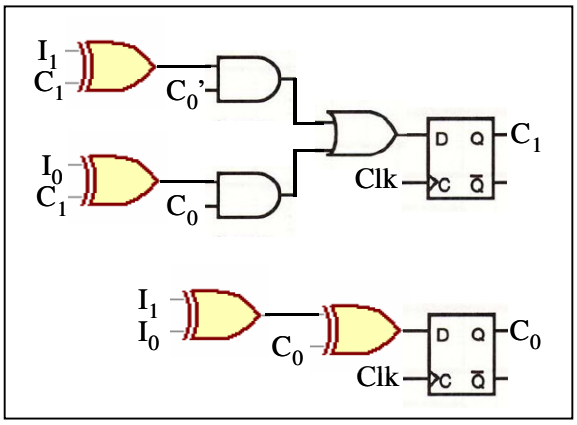
Problem 8. (BONUS) (10 points)
Draw the state diagram implemented by the circuit below. What does this circuit do?



Solution:

I1	I0	C1	C0	C1+	C0+
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	1	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	0	1	0	0
1	0	1	0	0	1
1	0	1	1	1	0
1	1	0	0	1	0
1	1	0	1	1	1
1	1	1	0	0	0
1	1	1	1	0	1

Stop counting

Count up by 1

Count down by 1

Count up by 2

I0, I1