An opamp schematic and its use as a switched-capacitor amplifier are shown below. All transistors are assumed to be biased in saturation region, and the opamp input node is properly biased. Use the following parameters: \( g_{m0} = \frac{1}{500} \Omega \) and \( r_o = 2k\Omega \) for NMOS transistor with \( W/L = 10 \) and biased with 1mA. PMOS mobility is \( \frac{1}{4} \) of NMOS mobility. Ignore all parasitics unless specified. Answer the followings assuming that \( M_1 \) through \( M_4 \) are sized to be \( W/L = 100 \), and biased with 100μA.

1. Estimate the DC loop gain of the feedback amplifier.

2. Estimate the closed-loop bandwidth of the amplifier.
3. Assume that the total parasitic capacitance at the source of $M_2$ is 0.16 pF, what is the phase margin?

4. Estimate the slew rate of this amplifier.

5. If a 1V step is applied to the input, how much does the output change after the amplifier settles?