Problem 1:

The circuit below is used to implement the function $Z = f(A, B) = \overline{A} + B$. $I$ and $J$ can be selected from the set $\{0, 1, B, \overline{B}\}$ ($B$ is the other input variable for the function $f$). What values should be chosen for $I$ and $J$? (10 points)

*Hint:* Express $Z$ as a function of $A$, $I$, and $J$. After that identify which values of $I$ and $J$ will produce $Z = f(A, B)$. 

![Diagram of circuit](image)
Problem 2: Develop a minimized Boolean implementation of a “one’s count” circuit that works as follows. The subsystem has four binary inputs: A, B, C, D; and generates a 3-bit output: XYZ. XYZ is 000 if none of the inputs are 1, 001 one input is 1, 010 if two inputs are 1, 011 if three inputs are 1, and 100 if all four inputs are 1.

(a) Draw the truth tables for X, Y, and Z.  
(b) Write down X, Y, and Z in canonical sum of products form.  
(c) Minimize the functions X, Y, Z using 4-variable K-maps. Write down the Boolean expressions for the minimized sum-of-products form of each function.
Problem 3: In many communication networking systems, the signal transmitted on the communication line uses a non-return-to-zero (NRZ) format. USB uses a specific version referred to as non-return-to-zero inverted (NRZI). A circuit that converts any message sequence of 0s and 1s to a sequence in NRZI format is to be designed. The mapping for such a circuit is as follows:

(a) If the message bit is 0, then the NRZI format message contains an immediate change from 1 to 0 or from 0 to 1, depending on the current NRZI value.

(b) If the message bit is 1, then the NRZI format message remains fixed at 0 or 1, depending on the current NRZI value.

This transformation is illustrated by the following example, which assumes that the initial value of the NRZI message is 1:

| Message:  | 10001110011010 |
| NRZI Message: | 10100001000110 |

(a) Find the Mealy model state diagram for the circuit. (15 pints)
(b) Find the state table for the circuit and make a state assignment. (10 points)
(c) Find an implementation of the circuit using D flip-flops and logic gates. (15 points)
**Problem 4:** Design a simple data path for the register transfers shown by the pseudo-code below, where X, Y, Z, W are four registers, and C1 and C2 are two control signals coming from the controller. Use a 4-to-1 multiplexer, with select signals s₀ and s₁. Assume the registers Y, Z, and W are connected to the 00, 01, and 10 input lines respectively of the multiplexer.

\[
\text{if } (C1 = 1) \\
\quad \text{then } X \leftarrow Y \\
\text{else if } (C2 = 1) \\
\quad \text{then } X \leftarrow Z \\
\quad \text{else } X \leftarrow W
\]

Draw the data path, showing the registers, the multiplexer, all the connections, and the multiplexer select signals. Derive the Boolean equations of the select signals s₀ and s₁ in terms of the control signals C1 and C2. 

(15 points)