Lecture 1.a
Class Introduction

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ECE 283 – Power Management Integrated Circuits (PMIC)

UCSD Jacobs School of Engineering

Hanh-Phuc Le

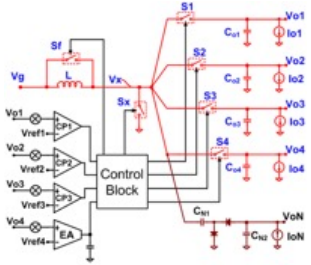
Assistant Professor, UC San Diego

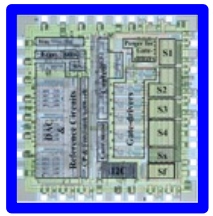
- **Ph.D.** **UC Berkeley, USA** **2013**
- **M.S.** **KAIST, Korea** **2006**
- **B.S.** **HUST, Hanoi, Vietnam** **2003**

- **Prior experience:**
  - University of Colorado Boulder 2016 – 2019
  - Lion Semi., San Francisco, CA 2012 – 2015
  - Rambus, Sunnyvale, CA 2012
  - Intel, Beaverton, OR 2009
  - Oracle, Santa Clara, CA 2008
  - JDA Tech., Korea 2004 – 2007
  - VAST, Vietnam 2002 – 2004

The Quest for iPower Circuits for All

SIMO (‘07-‘09)

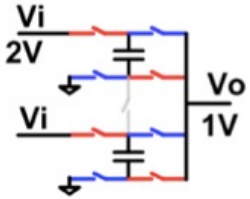


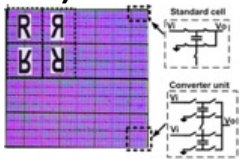


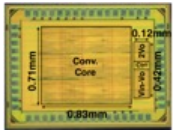
in LG SH150A (3G)

AMOLED Display Driver

SC – FIVR (‘10-‘13)



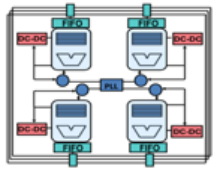


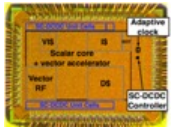


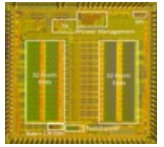
1st hi-perf. SC conv.

1W/mm², sub-ns response

Integ. Sys. and Func. (‘14-‘16)



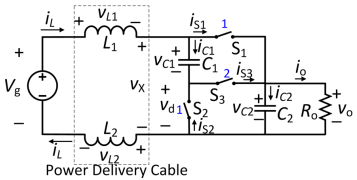




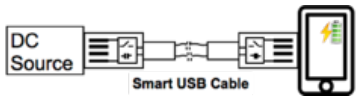
1st processor core with SC ripple conv.

iPower for brain implants

Hybrid Co . (‘13~)

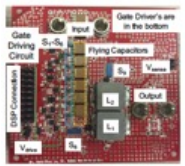


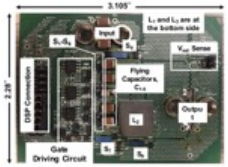
Integrate w/ Env. (‘17~)



material, smart architecture

High-V, Large Conv. (‘18~)





Class Logistics

- **All communications on Canvas**
  - Calendar
    - Zoom meeting link
  - Media Gallery
    - Class videos
  - Files
    - Lecture slides
    - CAD Tools materials
    - Assignments
  - Assignments and project reports
    - Online submission, PDF or PPT
  - Discussions
  - Grades
- **Log on remotely to campus servers to work on assignments and project**
  - You shall not copy/download any technology documents to your computer.
    - You will sign an NDA on this.
  - Access will be given to you in one week.

Class Contents

- **Learn power management design techniques in the integrated context**
- **DC-DC converter topologies and operations (2 weeks)**
  - Linear regulator, switched-inductor, switched-capacitor, and hybrid converters
  - Converter examples.
- **Loss optimization and power switch sizing (1 week)**
- **Analog and digital building blocks for power management ICs (2-3 weeks)**
  - Digital blocks: inverter, buffer, gate drivers, level shifter.
  - Analog blocks: Ramp and PWM generator, current mirror, amplifier, comparator, current sense, etc.
- **Stability and compensation (1 week)**
- **Other topics:**
  - Integrated devices introduction: integrated inductors, integrated capacitors
  - Pad ring and ESD protections
  - Bandgap reference circuits
  - Design examples

Prerequisites

- **Expected prior knowledge from classes below or equivalent**
  - ECE 102 Introduction to Active Circuit Design (required)
  - ECE 125A Introduction to Power Electronics I (highly recommended)
  - ECE 164 Analog Integrated Circuit Design (recommended)
  - ECE 165 Digital Integrated Circuit Design (Optional)

- **Familiarity with UNIX operating systems (CentOS/Redhat)**
  - Search for getting started tutorials as necessary

Expectation of Class Organization

- **Instructor: creates an environment.**
  - Provide background and practical design knowledge
  - Track student's learning process
  - Advise directions as well as detailed circuit designs

- **Students: take advantage of environment and setups**
  - Learn and innovate
  - Read technical papers, recommended books, and discuss
  - Not afraid of grades
  - Give feedback
  - Improve the environment for next generations.

Required Work and Grading

- **Quiz (sometimes in-class): 10%**
- **~4 Homework assignments: 25%**
  - Homework are all building blocks of the project.
- **Project: 65%**
  - Preliminary and intermediate reports: 30%
  - Final review & report: 35%
- **Term project has multiple phases, each has its own report/ presentation slide to submit.**

Project Reports

- **Project group:**
  - 3 students per group.
  - Teamwork
    - Specification definition: system level and block levels (team, possibly with a lead designer)
    - Sub-block assignment (parallel and individual)
    - Design integration (all team members)
- **Each group makes 3 oral presentation reports**
  - Preliminary design (in the week of Oct 25th)
  - Intermediate design review (in the week of Nov 15th)
  - Final design review (in the week of Nov 29th)
- **Final project report in PPT**
  - Update the final design review PPT with final simulation results Dec 1st.

Class Policy

- **Deadlines: beginning of lecture**
  - 50% penalty after 3 days
  - Submission closed after 1 week
- **Homework discussion is allowed and encouraged**
  - But must submit unique individual design.
- **Project sharing across teams**
  - Discussions and helping each others are encouraged
  - No sharing of actual circuit design is allowed
    - Possible collaboration is limited to sharing skill scripts or similar
- **All students are bound by the UCSD Academic Integrity**

Software

- **Cadence Virtuoso**
  - Increasingly popular in industry
  - Lots of online tutorials and documentations
- **Start reading Cadence to prepare**
  - Canvas >> Files >> CAD Tool - Cadence
- **Will have the first HW/lab on starting Cadence.**
  - Should be very simple with all the presets prepared.
    - Need to contact Prof. Le to resolve problems of software ASAP.