ECE SRIP

FACULTY MENTOR
Rosing, Tajana

PROJECT TITLE
Accelerating bioinformatics workloads

PROJECT DESCRIPTION
Genomic data is doubling every seven months and is expected to surpass YouTube and Twitter rate by 2025. Standard microbiome pipeline starts with RNA/DNA sequencing, passes through a preprocessing step (trimming and alignment), and followed by downstream analysis. The daily-generated data can reach 10 TB and needs expensive operations such as alignment which takes months to process and is prohibitive for real-time hospital setup and personalized diagnostic and prescription. The main aim of this project is end-to-end acceleration of the genomic pipeline using commercial off-the-shelf accelerators such as FPGAs and GPUs, while also profiling available toolsets/algorithms to reveal bottlenecks to potentially realize a specialized chip, e.g. ASIC or processing-in-memory (PIM) or in-storage. In addition to stand-alone accelerator cores, we are also looking for a genomic cluster (e.g. a homogeneous fully-FPGA cluster or a heterogeneous system comprising FPGA, GPU, PIM, etc.) capable of processing 10 TB and larger data in a systematic and efficient way. The project also involves devising new algorithms or augmenting the available algorithms to make them suitable for the targeted hardware (FPGA, GPU, and PIM in the future).

Remote

INTERNS NEEDED
2

PREREQUISITES
Experience with FPGA (HLS) or GPU or ASIC/PIM design, computer architecture/VLSI knowledge

FACULTY MENTOR
Rosing, Tajana

PROJECT TITLE
Hyperdimensional computing systems design

PROJECT DESCRIPTION
Hyperdimensional (HD) Computing has been shown to be robust to various types of computing errors ranging from wireless communication to bitflips during computing. Additionally, HD utilizes high dimensional bit-level operations that offer high levels of parallelism that can be accelerated with Processing-in-Memory (PIM) architectures, using emerging technologies such as ReRAM cells. Emerging computing technologies often have inherent errors in data representation during computing. For instance, the values stored as conductances in ReRAM cells are inaccurate. However, with the robust property of HD computing, we can utilize the benefits of these emerging technologies without impacting the accuracy of HD computing as it is robust to the representation errors that occur in emerging computing technologies. Additionally, we can take further advantage of the robust property of HD and gain further energy efficiency by voltage overscaling. This project would mostly encompass modeling the errors of various emerging computing technologies for PIM in software and testing their impact on the accuracy of HD.

Remote

INTERNS NEEDED
1

PREREQUISITES
Experience with ASIC/PIM design, computer architecture/VLSI knowledge
Experience with Python

FACULTY MENTOR
Rosing, Tajana

PROJECT TITLE
Acceleration of Fully Homomorphic Encryption in PIM

PROJECT DESCRIPTION
Homomorphic encryption is an encryption scheme that allows to evaluate arbitrary functions on encrypted data without a need to decrypt. This magic ability to execute computation on encrypted data comes with severe performance and storage overheads, and limitations in the complexity of the function to evaluate for each given choice of the encryption parameters. Evaluating functions of arbitrary complexity requires the deployment of the techniques to refresh the noise accumulated in the ciphertexts during the evaluation of a function, especially multiplications. While useful,this is an extremely expensive procedure that increases the critical path of a function evaluation. In this proposal, we aim to design an extremely efficient FHE acceleration platform around the concept of processing in memory (PIM). The use of PIM mitigates data expansion overhead in homomorphic encryption, increases the amount of parallelism that can be exploited at once while processing ciphertexts, it minimizes data movements of ciphertexts, hence, it promises to greatly improve performance of private computation greatly with respect to software implementations on CPU and other existing accelerators.

Remote

INTERNS NEEDED
1

PREREQUISITES
Experience with GPU or ASIC/PIM design, computer architecture/VLSI knowledge